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Large-scale flexible and transparent electronics based on monolayer molybdenum disulfide field-effect transistors

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Atomically thin molybdenum disulfide (MoS_2) is a promising semiconductor material for integrated flexible electronics due to its excellent mechanical, optical and electronic properties. However, the fabrication of large-scale MoS_2-based flexible integrated circuits with high device density and performance remains a challenge. Here, we report the fabrication of transparent MoS_2-based transistors and logic circuits on flexible substrates using four-inch wafer-scale MoS_2 monolayers. Our approach uses a modified chemical vapour deposition process to grow wafer-scale monolayers with large grain sizes and gold/titanium/gold electrodes to create a contact resistance as low as 2.9 kΩ μm^{-1}. The field-effect transistors are fabricated with a high device density (1,518 transistors per cm^2) and yield (97%), and exhibit high on/off ratios (10^{10}), current densities (~35 μA μm^{-1}), mobilities (~55 cm^2 V^{-1} s^{-1}) and flexibility. We also use the approach to create various flexible integrated logic circuits: inverters, NOR gates, NAND gates, AND gates, static random access memories and five-stage ring oscillators.

Flexible electronics is of use in a wide range of applications including wearable sensors, e-skins, flexible displays and energy converters[1–7]. An important trend in the field is the development of high-performance electronics on large scales[8–12]. Approaches based on organic molecules have been researched widely[3,13–17], but usually suffer from low device performance and non-compatibility with standard fabrication technology. Carbon nanotubes[11,18–21], semiconductor nanowires[10,22], zinc oxide (ZnO) thin films[23–25] and multilayer indium selenide (InSe)[26] have also been explored and offer promising capabilities. However, their fabrication scale and low device yield limit their practical applications.

Recently, attention has switched to the use of two-dimensional (2D) semiconductors in flexible electronics due to their atomic thicknesses as well as excellent electrical, optical and mechanical properties[5,7,27–30]. 2D semiconductors, and molybdenum disulfide (MoS_2) in particular, can be fabricated at electronic grade (wafer-scale and high-quality)[31–34], and individual MoS_2 field-effect transistors (FETs) fabricated on rigid substrates have shown high on/off ratios (around 10^8), high mobilities (167 ± 20 cm^2 V^{-1} s^{-1}) and steep subthreshold swings (74 mV dec^{-1})[35,36]. MoS_2 is also attractive for constructing integrated circuits, and various logic circuits have been demonstrated on rigid substrates[34,37]. Furthermore, flexible FETs and circuits based on exfoliated few-layer MoS_2 have been created and shown to exhibit high performance[38]. However, due to materials and process limitations when fabricating on flexible substrates, only primitive circuits, involving no more than three discrete MoS_2 transistors, have so far been created on flexible substrates[39,40].

In this Article, we report the fabrication of four-inch-wafer-scale transparent MoS_2 FET arrays on polyethylene terephthalate (PET) substrates. We use a layer-by-layer fabrication process to create flexible and clean MoS_2 transistor arrays that exhibit excellent device-to-device uniformity, a device density of 1,518 transistors per cm^2 and a yield of 97%. The devices exhibit on/off ratios of ~10^{10}, current densities of ~35 μA μm^{-1}, carrier mobilities of ~55 cm^2 V^{-1} s^{-1} and good stability and strong tolerance under strain. This scalable fabrication of high-performance transistor arrays (with 54,640 transistors per wafer) enables the production of large-area flexible integrated multistage circuits, and we demonstrate circuits for inverters (with voltage gain as high as 107 at $V_{dd} = 4$ V), NOR gates, NAND gates, AND gates, static random access memories (SRAMs) and five-stage ring oscillators.

Scalable assembly of MoS_2 flexible electronics

Our large-scale devices were fabricated from 4-inch monolayer MoS_2 wafers (inset, Fig. 1a), which were grown by epitaxy techniques we developed previously[31,41]. To scale up the wafer size from the previously used 2 inches (ref. [31]) to 4 inches, we redesigned our chemical vapour deposition (CVD) system by enlarging the growth chamber and adding more evaporation cells for sulfur and molybdenum oxide. The carrier gases in each evaporation cells were independently flowed so as to achieve evaporation control and stability. Moreover, sapphire substrates were loaded into our growth chamber with wafer surfaces facing directly to the evaporation cells to guarantee a steady mass flux transportation of precursors to the 4-inch sapphire substrates. As a result of such new growth design, fully covered (Supplementary Fig. 1a), wafer-scale and high-quality monolayer MoS_2 was epitaxially grown on sapphire with only two crystalline orientations: 0° and 60°.

Figure 1b,c shows optical images of partially and fully covered samples after 20 and 40 min of growth, respectively. A typical

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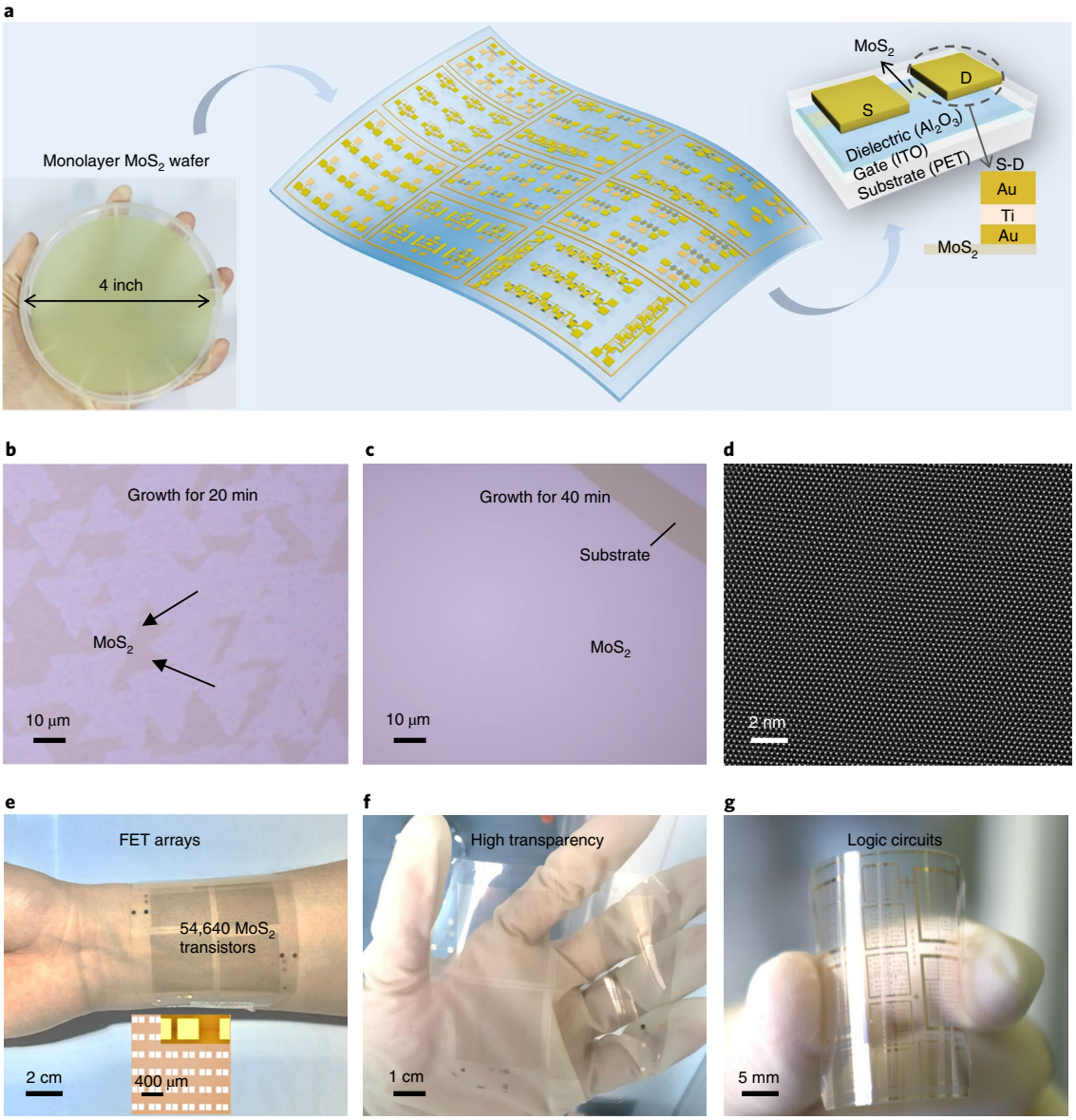

Fig. 1 | Schematic and fabricated MoS_2 transistor devices on flexible substrates of PET. a, Illustration of flexible transistor arrays with integrated circuits. Left inset: the 4-inch monolayer MoS_2 wafer grown by epitaxy techniques. Right inset: the specific structure of the flexible MoS_2 FETs. **b**, Optical image of MoS_2 domains grown on a 4-inch sapphire substrate for 20 min; the side length of the triangular MoS_2 domain is ~20 μm. **c**, Optical image of a continuous monolayer MoS_2 film grown for 40 min. **d**, HRTEM image of the as-grown monolayer MoS_2. **e**, Photograph of very large-scale flexible MoS_2 transistor arrays with a device density of 1,518 transistors per cm^2, completely fitted to a human wrist. Inset: magnified image of FET arrays. **f**, Photograph of the flexible MoS_2 transistor arrays, showing their outstanding optical transparency. **g**, Photograph of various integrated multistage circuits on flexible substrate, including inverters, NOR gates, NAND gates, SRAMs, AND gates and five-stage ring oscillators.

high-resolution transmission electron microscopy (HRTEM) image of the as-grown sample is shown in Fig. 1d, demonstrating a nearly perfect lattice structure with very low defect density. Atomic force microscope (AFM), Raman and photoluminescence (PL) characterizations are presented in Supplementary Fig. 1b–d. Compared with our previous samples with smaller grain sizes (~600 nm in ref. [41] and ~1 μm in ref. [31]), the present monolayer MoS_2 samples have much larger grain sizes (~20 μm on average). They thus should have higher quality due to the notably decreased density of grain boundaries, as is illustrated in the device characterization discussed in the following.

These wafer-scale MoS_2 monolayers (serving as the semiconductor layer) on sapphire were transferred onto PET substrates pre-deposited with 30-nm indium tin oxide (ITO, serving as the back-gate electrode layer) and 35-nm aluminium oxide (Al_2O_3, serving as the dielectric layer) on top to enable further device fabrications. Standard UV lithography, metal film deposition and a lifting off process were performed for the fabrication of devices. Au(3 nm)/Ti(3 nm)/Au(30 nm) were used for source/drain contact electrodes to achieve good electrical contact (top right inset of Fig. 1a). In previously fabricated large-scale flexible devices, particle contamination and residues were usually present[13,18,42] and could degrade device performance and yield. For the ultra-thin 4-inch monolayer MoS_2, which is easy to pattern using a planar process, we employed a layer-by-layer fabrication process to avoid contamination or bubbles (for more details see Supplementary Figs. 2, 3, 4

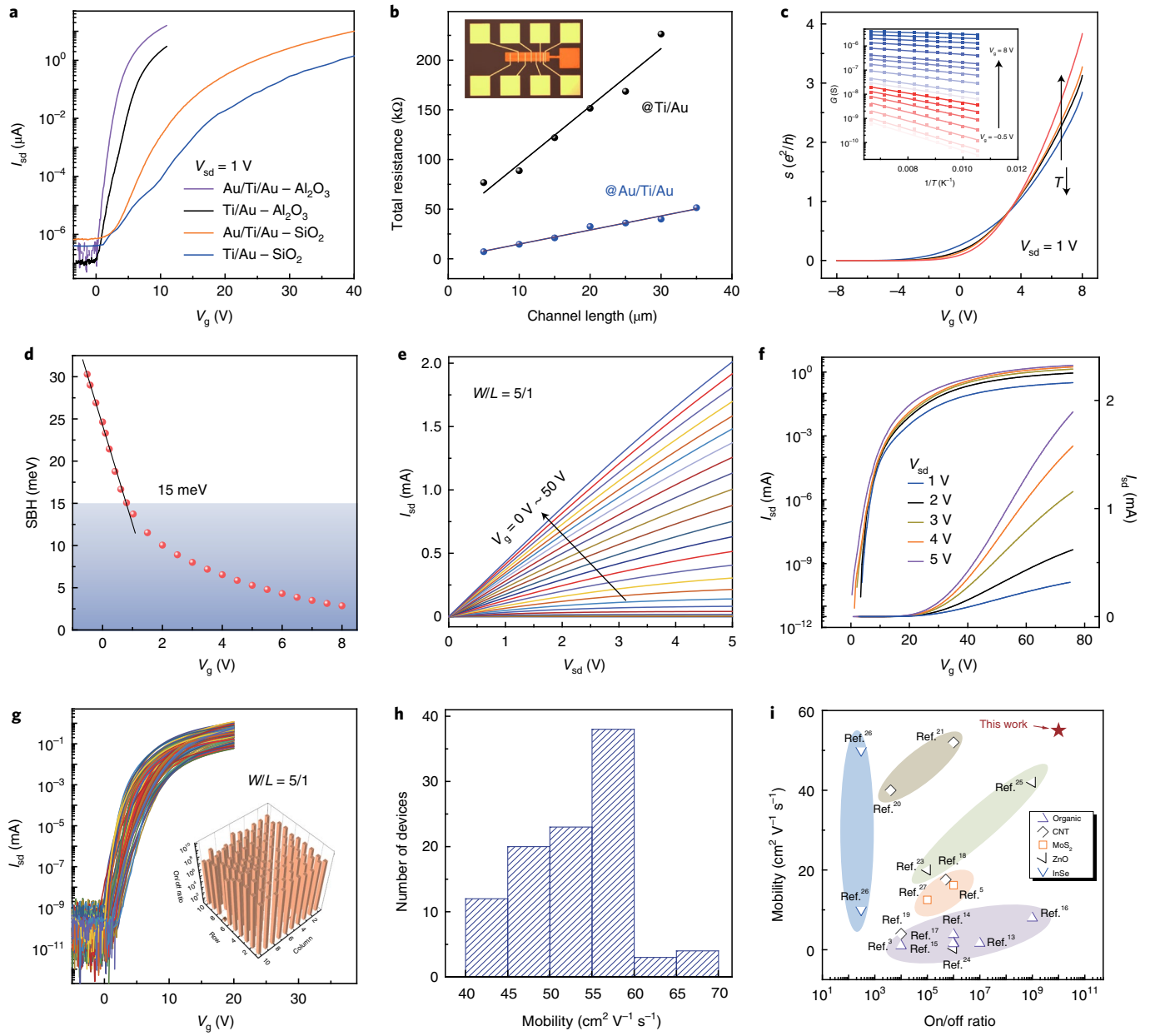

Fig. 2 | Performance characterization of the MoS_2 transistors. a, I_{sd}–V_g curves of MoS_2 FETs with different metal contacts and dielectric layers. **b**, Transfer-length-method (TLM) measurements of the contact resistance from the Ti/Au and Au/Ti/Au electrodes. **c**, Transfer curves of Au/Ti/Au contacted devices measured at various temperatures, where *s* is sheet conductivity. Inset: Arrhenius plot at different V_g. **d**, V_g dependence of the SBH for monolayer MoS_2 transistors with Au/Ti/Au contacts. **e**, I_{sd}–V_{sd} output characteristics of a device with channel width and length of 30 and 6 μm, respectively. **f**, Corresponding I_{sd}–V_g transfer characteristics at different bias voltages. **g**, Transfer curves at V_{sd} = 3 V for 97 flexible MoS_2 FETs in the 100-transistor array. Inset: on/off ratio map for each transistor location. **h**, Statistics of mobility from 100 flexible transistors. **i**, Summary of the on/off ratio and mobility for various large-area flexible transistors reported in the literature.

and 11) and could achieve clean MoS_2 devices with a high yield and scalable production.

Figure 1a illustrates the large-scale flexible MoS_2 transistor arrays and integrated multistage circuits. Several as-fabricated samples are shown in Fig. 1e–g. Figure 1e shows a typical flexible MoS_2 transistor array on PET with a total of 54,640 devices. Compared with previous reports[3,13], an improved device density of 1,518 per cm^2 has been achieved. The aligned elements of flexible MoS_2 transistors with different channel lengths and widths can be clearly seen in the inset of Fig. 1e. Moreover, these devices, fabricated on PET substrates, show high transparency (Fig. 1f and Supplementary Fig. 5). To highlight the versatility of our approach, various flexible logic circuits implementing different functions were demonstrated, including inverters, SRAMs, NOR gates, NAND gates, AND gates and five-stage ring oscillators, by integrating individual devices (Fig. 1g).

High-performance flexible MoS_2 FETs

The contact resistance between the semiconductor channel and metal electrodes is well known to strongly affect device performance[35,43]. Here, the Au/Ti/Au contacts provide a very low contact resistance for monolayer MoS_2 FETs. The titanium layer was used to improve adhesion between the electrodes and underneath the MoS_2.

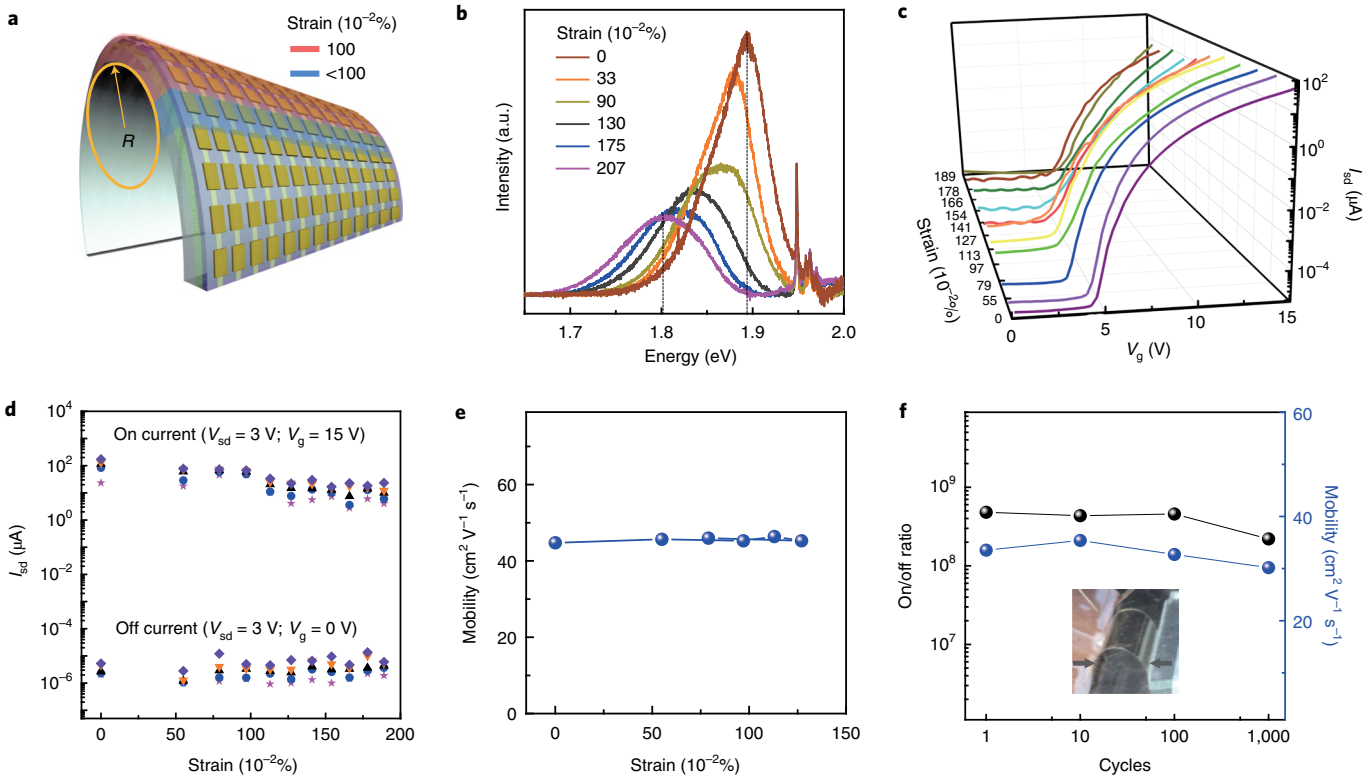

Fig. 3 | Electrical performance of flexible devices under strain. a, Schematic of the strain distribution of flexible MoS_2 transistor arrays under bending. **b**, PL spectra of monolayer MoS_2 under different tensile strains. **c**, I_{sd}–V_g transfer curves of flexible MoS_2 transistors (L/W = 3:1) at different strains. **d**, On and off currents of five randomly picked devices versus strain. **e**, The dependence of charge-carrier mobility on strain. **f**, On/off ratio and charge-carrier mobility of a device subjected to 10^3 cycled tests of bending and releasing. Data were measured at 1% strain. Inset: photograph of flexible devices at 1% strain.

Note that the bottom gold layer in the Au/Ti/Au contact is just a few nanometres thin and it would be very difficult to form a continuous film during evaporation considering the perfectness and inertness of the MoS_2 surface. It is thus most likely that the middle titanium layer is mixed with the bottom gold layers during evaporation, while also maintaining good adhesion and good ohmic contact between the electrodes and MoS_2. I_{sd}–V_g (source–drain current versus gate voltage) curves of devices fabricated on different dielectric layers and with different metal contacts are shown in Fig. 2a. It can be seen clearly that the Au/Ti/Au contacted devices have higher on/off ratios and smaller subthreshold swing (SS). The measured contact resistance of the Au/Ti/Au contacted devices is only 2.9 kΩ μm, over 10 times smaller than that of Ti/Au contacted devices (Fig. 2b). The devices' contact resistances were extracted by using the transfer length method[44]. The Schottky barrier height (SBH) between the contact and MoS_2 channel was also extracted from Arrhenius plots (Fig. 2c). The reported SBH is ~50–350 meV for Ti/Au contacts[45,46] and 15 meV for the present Au/Ti/Au contacts (Fig. 2d). Such SBH is among the lowest values for various contacts for monolayer MoS_2 (refs. [46,47]), suggesting Au/Ti/Au is an excellent contact structure to reduce contact resistance in monolayer MoS_2 devices. This is discussed further in Supplementary Section 4.

In our device structure, an Al_2O_3 layer on ITO was deposited via a modified atomic layer deposition (ALD) process[48] and shows excellent dielectric properties, manifested by the ultra-low gate leakage current of $I_{gs} < 200$ fA at V_g varying from −10 V to 70 V (Supplementary Fig. 6). Figure 2e,f shows the output (I_{sd}–V_{sd}) and transfer (I_{sd}–V_g) curves of a typical transistor with channel width/length (W/L) of 30/6 μm. An extremely high on/off ratio of 10^{11} has been observed. These device performances are comparable to the best reported on rigid substrates[35]. We also characterized the on/off ratio distribution for a typical 10 × 10 transistor array (Fig. 2g), showing good uniformity. The transfer curves of these devices show little device-to-device variations with an overall yield of 97% with small hysteresis (Supplementary Fig. 7). Based on transfer curves and the capacitance of the Al_2O_3 dielectric layer (Supplementary Fig. 8), we derived an average charge-carrier mobility of ~55 $cm^2 V^{-1} s^{-1}$ for these devices at $V_g \approx 20$ V (Fig. 2h). Generally, for large-scale flexible transistors, organic semiconductors exhibit relatively low carrier mobilities (~0.1–10 $cm^2 V^{-1} s^{-1}$)[13–17]. Although carbon nanotubes demonstrate high mobilities, the on/off ratios have an undesired tradeoff with channel length due to the presence of metallic tubes[18–21]. In Fig. 2i and Supplementary Table 1 we compare the on/off ratio and mobility with those of previously reported large-scale flexible transistors, showing that our monolayer MoS_2 device performances are very promising. Moreover, time stability was established by showing that the device performance is basically maintained at the same level after being left in the atmosphere for 30 days (Supplementary Fig. 9).

To explore the mechanical performances of our flexible MoS_2 transistors, we performed convex bending tests (Fig. 3a). Here, the largest bending corresponds to a tensile strain of 2%. Figure 3b presents the strain-dependent fluorescence spectra of our MoS_2 samples. When increasing the strain, the A-exciton peak is red-shifted and reduced in intensity. This change is consistent with a transition of the optical bandgap of MoS_2 from direct to indirect at strain >1% (ref. [49]). Mechanical strain in MoS_2 can also affect its optical bandgap, quantum emission properties and electrical properties[50]. However, in our bending test, the electrical performance of the MoS_2 transistors was well preserved under strain up to ~1% (Fig. 3c), consistent with previous works[51]. Figure 3d shows the on- and off-current distributions for five devices in different regions when

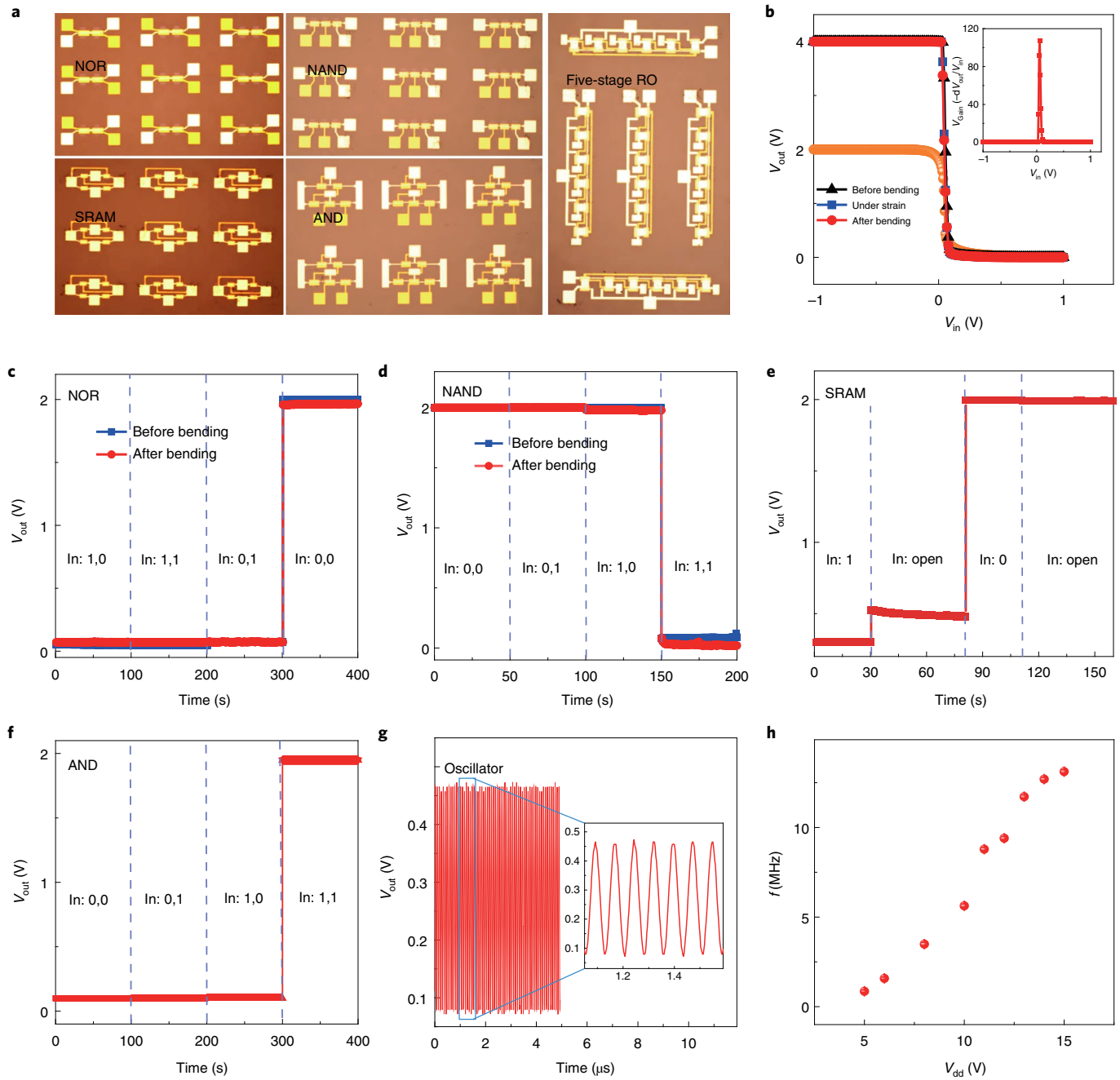

Fig. 4 | MoS_2-based flexible logic gates and oscillators. a, Photographs of different MoS_2 integrated devices on flexible substrates. **b**, Output voltage of an inverter as a function of input voltage when under different bending states. Inset: voltage gain of the inverter under an input of 4 V. **c**,**d**, Output characteristics of flexible NOR (**c**) and NAND (**d**) gates before and after bending at V_{dd} = 2 V. Logic '0' and '1' mean 0 V and 5 V, respectively, for these and all the following logic devices. **e**,**f**, Output characteristics of flexible SRAM (**e**) and AND (**f**) gates at V_{dd} = 2 V. **g**, Output waveform of a five-stage ring oscillator at V_{dd} = 15 V. **h**, Output frequency as a function of supply voltage V_{dd}. Error bars represent one standard deviation.

applying strain from 0 to 2%. Below a strain of 1.13%, off/on currents show no obvious increase/decrease and the device performances can be largely preserved (Fig. 3e). Previous finite-element method analysis revealed that the devices' active layers, MoS_2 and Al_2O_3, experienced strain far less than their failure level when the fabricated device arrays were bent into folded states[5]. Furthermore, these flexible devices are also tolerant to multiple bending tests (>10^3 cycles), with the on/off ratio and mobility remaining at the same level (Fig. 3f). These results prove the reliability of our MoS_2 transistors, which is important for building high-performance flexible electronics.

Performance characteristics of large-scale flexible logic circuits

To further demonstrate the diversity of such MoS_2 transistors, we fabricated integrated flexible logic devices, such as inverters, NOR gates, NAND gates, SRAMs, AND gates and five-stage ring oscillators by integrating 2, 2, 3, 4, 5 and 12 transistors, respectively (Fig. 4a and Supplementary Figs. 10 and 11). Note that ITO acting as the local bottom gate is not compatible with UV lithography and subsequent electrical measurements because of its invisibility (that is, high transparency). Accordingly, we chose a Ti/Au gate instead

of the ITO gate to fabricate flexible logic devices. Flexible FETs with Ti/Au local bottom gates have no noticeable differences in performance when compared with ITO global gates (Supplementary Figs. 12–14).

Figure 4b and Supplementary Fig. 15 show the typical electrical characteristics of an inverter; high voltage gains of 43 and 107 at bias voltages of $V_{dd}=2$ V and 4 V can be achieved, respectively. This high voltage gain is several times higher than the previously reported values for MoS_2-based inverters both on rigid and flexible substrates[34,37–39] and also comparable to flexible inverters constructed on other materials (Supplementary Fig. 16a). Moreover, the voltage swings of our flexible inverters are also tolerant to strain. Two essential logic gates—NOR and NAND gates—are shown in Fig. 4c,d. The outputs are in two states—0 V and 2 V—by combining two input voltages ('0'/'1') logically at $V_{dd}=2$ V and are stable after bending. Here, logic '0' and '1' mean 0 V and 5 V, respectively (this also applies to the SRAM, AND and NAND logic devices discussed hereafter). Based on these basic logic functions, more complex logic devices can be designed. Figure 4e shows the characteristics of a flip-flop memory cell (SRAM) consisting of two inverters coupled to storage nodes. This SRAM cell has two stable output states—0 V and 2 V at $V_{dd}=2$ V. At 30 s and 110 s, the input has opened while the output of this flip-flop cell remains at states 0 V and 2 V. Figure 4f shows the characteristics of an AND gate constructed from a NAND gate and an inverter at $V_{dd}=2$ V. This can be set to state 0 V or 2 V by modifying the two input voltage states.

We next demonstrate a flexible ring oscillator based on monolayer MoS_2. These five-stage ring oscillators are integrated by cascading five inverters and an additional inverter as output buffer to eliminate interference. In each ring oscillators, the component FET devices have a device scaling of $W=3$ μm, $L=3$ μm and a gate dielectric thickness of 35 nm. Figure 4g shows the characteristics of a typical oscillator. Benefiting from the smoothness and cleanness of our devices (Supplementary Figs. 4, 11 and 12), our flexible ring oscillator achieves high oscillation frequency (f) and fast stage delays (τ). A stable oscillation frequency of 13.12 MHz at $V_{dd}=15$ V, corresponding to a stage delay of $\tau=1/(2Nf)=7.6$ ns in the flexible ring oscillator (where N is the number of inverter stages), can be achieved. This value is comparable to current state-of-the-art flexible ring oscillators made of various semiconductor materials (Supplementary Fig. 16b). Additionally, the output frequency of the ring oscillator can be adjusted by varying the supply voltage, V_{dd} (Fig. 4h). Oscillation frequencies of 860 kHz and 13 MHz were obtained when applying $V_{dd}=5$ V and $V_{dd}=15$ V, respectively.

Conclusions

We have reported the large-scale fabrication of flexible electronic devices with high device yield, density and uniformity using four-inch-wafer-scale monolayer MoS_2. The individual devices exhibit large on/off ratios, high mobilities, high current densities and excellent flexibility. We also created integrated flexible devices for multistage logic circuits. Our work provides a method for fabricating large-scale flexible integrated MoS_2 devices that could be of value in the development of flexible electronics for applications in computing, communications, sensing and information storage.

Methods

Epitaxial growth of MoS_2. The MoS_2 growth was performed in a 4-inch CVD chamber. Sulfur (Alfa Aesar, 99.9%, 10 g) and MoO_3 (Alfa Aesar, 99.999%, 60 mg) powders were used as reaction sources. Pre-annealed 4-inch sapphire wafers with clean and atomically flat surfaces were used as substrates. During the growth, the tubes loaded with S were flowed with Ar (gas flow rate, 40 s.c.c.m.) and the tubes loaded with MoO_3 were flowed with Ar/O_2 (gas flow rate, 180/3 s.c.c.m.). The temperatures for the S, MoO_3 and substrate zones were 115, 540 and 930 °C, respectively. For a typical growth run, the pressure in the chamber was ~1 torr and the growth lasted for ~40–60 min.

Transfer of wafer-scale MoS_2. First, 5% 950 polymethyl methacrylate (PMMA) in anisole was spin-coated on MoS_2/sapphire at a speed of 2,000 r.p.m. then baked at 180 °C for 1 min. This process was repeated three times. Second, as-made PMMA/MoS_2/sapphire samples were immersed in KOH solution at 110 °C for half an hour. The samples were then picked up from the solution and transferred into deionized water to release the PMMA/MoS_2 layer from the sapphire. After full release, the PMMA/MoS_2 layers floated to the surface of the deionized water and could be picked up and transferred to targeting substrates. Finally, transferred samples were kept at room temperature for ~12 h to remove the extra water. The PMMA was washed out in acetone.

Fabrication of flexible MoS_2 devices. As shown in Supplementary Fig. 2, 30-nm-thick ITO was first deposited on the PET substrate by magnetron sputtering. An ALD system was then used to deposit 35-nm-thick Al_2O_3 on the PET/ITO at 110 °C with H_2O and trimethyl aluminium as precursors and high-purity N_2 as the carrying gas. The monolayer MoS_2 was transferred onto PET/ITO/Al_2O_3 substrates, then UV lithography (MA6, Karl Suss) and reactive ion etching (Plasma Lab 80 Plus, Oxford Instruments) were used to define MoS_2 channels with AR-5350 as the photoresist, which was spin-coated on the sample surface at 4,000 r.p.m. and baked at 100 °C for 4 min. Au(3 nm)/Ti(2 nm)/Au(30 nm) were deposited on the MoS_2 channels as source–drain electrodes by electron beam evaporation followed by a second UV lithography process. For the flexible MoS_2 logic circuits, fabrication started with patterning of the separated bottom metal layer by UV lithography and evaporation of Ti (2 nm)/Au (13 nm) on a PET substrate, then 35 nm of Al_2O_3 was deposited by ALD as the dielectric layer. The next steps were conducted following the same fabrication process as for MoS_2 FET arrays.

Characterizations and measurements. Raman shift and PL characterizations were performed on a JY Horiba HR800 system with a laser excitation wavelength of 532 nm and power of 0.6 mW. Surface imaging of these samples was carried out with an AFM (Veeco Multimode III). Electrical measurements were performed in a probe station and under dark conditions with semiconductor parameter analysers (Agilent 4156C and B1500).

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

G.Z. supervised the project. Q.W. performed the growth of the 4-inch MoS_2 wafers. N.L. fabricated the flexible devices with help from Z.W., H.Y., C.S., J. Zhao. and G.W. N.L. performed the electrical measurements with help from C.S. and X.L. N.L., Q.W., R.Y. and G.Z. analysed data. N.L., Q.W., C.S., R.Y. and G.Z. wrote the manuscript and all authors commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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